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(54) **Multipurpose, internally configurable integrated circuit for driving in a switching mode external inductive loads according to a selectable connection scheme.**

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(73) Proprietor : **SGS-THOMSON MICROELECTRONICS s.r.l.**
Via C. Olivetti, 2
I-20041 Agrate Brianza Milano (IT)

(72) Inventor : **Rossi, Domenico**
Via Roma, 161
I-27024 Cilavegna (IT)
Inventor : **Cuomo, Andrea**
Viale Beatrice d'Este, 40
I-20122 Milano (IT)
Inventor : **Pietrobon, Giovanni**
Via Steffani, 18
I-31100 Treviso (IT)

(74) Representative : **Pellegri, Alberto et al**
c/o Società Italiana Brevetti S.p.A.
Via Puccini, 7
I-21100 Varese (IT)

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Description

BACKGROUND OF THE INVENTION

1. Field of the invention

The present invention relates to an integrated circuit which may be internally configured by programming, for controlling the switching of a driving current through a single or multiple inductive loads connected across output terminals of the integrated device in accordance with one of several different connection schemes which may be selected for a particular application.

2. Description of the prior art

The controlled driving of stepping motors, transformers, electromagnets and similar actuating means, typically representing inductive loads, is commonly implemented by employing an integrated device combining the output power transistors (typically four power switching transistors connected to a virtual ground node which are referred to as "low-side drivers" and one or more often two power switching transistors connected to the supply rail, known as "high-side driver(s)") and a driving circuit. The latter typically includes a pulse-width-modulation (PWM) control loop, driven by a clock signal, which controls the "duty-cycle" of driving signals fed to the output power switching transistors in function of the detected value of the current flowing through the external load and of a control reference voltage.

Integrated circuits of this kind are well known to a skilled technician and may take different forms, more or less advantageous under certain aspects, but which essentially remain based upon PWM control loops. Among these types of circuits, particularly advantageous is a control circuit based upon a current sharing principle described in the pending European Patent Application Number 88115444.7, filed on September 21, 1988 and claiming a Convention priority date of October 5, 1987, wherein by employing a single current sensing resistor for the current flowing through the external loads, it is possible to adjust independently the current flowing through two external loads connected according to a "dual-half-bridge" scheme or according to a "unipolar motor" connection scheme. The description of such a switching control circuit is here incorporated. On the other hand, the kind of the external inductive load or loads to be driven by the integrated circuit, whether represented by an unipolar motor or by one or more unidirectional motors, solenoids, etc., normally requires a specific design of the integrated switching control circuit compatible with the particular drive configuration or connection scheme of the external load or loads to be driven. In the accompanying Figures 1a, 1b, 1c and 1d, several well known driving schemes for inductive loads (L), according to a bridge, dual-half-bridge, electromagnet, and unipolar motor drive configuration are respectively depicted. In these illustrations six power switching transistors indicated with HSD1, HSD2 (i.e. the two High-Side Drivers), LSD1, LSD2, LSD3 and LSD4 (i.e. the four Low-Side Drivers), respectively, are shown, each being provided with a power diode for the recirculation of the discharge current of the relative external inductive load L. In case of driving an electromagnet, as depicted in Fig. 1c, the integrated circuit may contain also two additional recirculation diodes D1 and D2 as it is well known to a skilled technician. In all the examples shown, a single sensing resistor (Rsense), connected between a virtual ground node and the real ground of the supply circuit, is shown. Obviously the use of a single sensing resistor in the case of the circuit of Fig. 1b, i.e. a dual-half-bridge drive configuration for two external loads L and L', necessarily requires a current sharing kind of switching control circuit when an individual control of the two loads is desired, as described in the above cited application.

According to the prior art, the integrated circuit for controlling the switching must essentially be designed specifically for the contemplated application, e.g. a bridge type application (Fig. 1a), a unipolar motor application (Fig. 1d), and so forth.

An approach to provide a "multipurpose" power driver system that can be adapted for employment in various types of application, requiring any one of different bridge modes or unipolar mode of operation is disclosed in EP-A-0 198 248. The system proposed comprises a power driving unit, to which a certain external load or a plurality of external loads may be connected through a plurality of ouput pins of the power driving unit. A supervising microprocessor provided with an appropriate program, a certain portion of which may be selected by the user according to need, controls the driving of a set of power switching elements of the control unit. Synchronization, current adjustment, and up to 27 different possible configurations of the power switching unit may be implemented by preselecting the desired routine to be executed by the controlling microprocessor. The vast range of modes of operation selectable by programming must pay off the relative complexity (cost) of the system that requires a microprocessor, an electrically programmable and erasable read-only memory (EEPROM), and a power driving integrated device interconnected by a control bus.

Therefore it would be of great utility the availability of an integrated device for controlling the switching of a drive current across external inductive loads (single or multiple loads), which could be internally configured so as to be usable for a driving scheme selectable among a number of possible driving schemes of the externally connected load or loads.

OBJECTIVE AND SUMMARY OF THE INVENTION

The main objective of the present invention is that of providing an integrated circuit for controlling the switching which may be internally configured by means of selection logic means which may be controlled by the user for making the control circuit functionally suited for a certain driving scheme of an external load or loads which may be implemented by suitably bridging output terminals of the integrated circuit and connecting the external load or loads thereto.

This and other objectives and advantages which will emerge during the following description, are achieved by the switching mode, driving circuit of the invention, which may also conveniently use a single PWM control loop utilizing a single sensing resistor connected between a virtual ground node to which four "low-side drivers" are connected and the real ground of the supply circuit and which is capable of generating at least a control signal, the "duty-cycle" of which is determined by means of a clock signal and a reference voltage. This control signal generated by the PWM control loop is substantially fed to the input of a configurable logic circuit, which may comprise a read-only memory (ROM) and/or a similarly programmable logic array (PLA) and suitable selection registers (programming registers). The configurable logic circuit produces as many drive signals for as many output power switching transistors are used (i.e. for the four "low-side drivers" and for the unique or for the two "high-side drivers") in conformity with a selected driving scheme to be implemented.

According to a preferred embodiment of the invention, the use of relatively slow ROM or PLA, i.e. with a relatively long access time, is made possible without such a speed limit of the programmable logic circuit having a negative effect upon the correct driving in a switching mode of the external load or loads.

BRIEF DESCRIPTION OF THE DRAWINGS

Figures 1a, 1b, 1c and 1d depict as many driving schemes of one or more external loads which are commonly adopted in the art, as described above;

Figure 2 is a basic block diagram of the integrated driving circuit of the present invention;

Figure 3 is a block diagram of an embodiment of the circuit of the invention suitable to utilize programmable devices having a relatively long access time;

Figure 4 is a circuit diagram of one of the blocks of the diagram of Fig. 3;

Figure 5 is a more detailed functional block diagram of a circuit of the invention.

DESCRIPTION OF PREFERRED EMBODIMENTS

A basic block diagram of the integrated driving circuit of the invention is depicted in Fig. 2. The two power devices connected to the supply rail Vs, i.e. the two "high-side drivers" HSD1 and HSd2, and the four power devices which are connected to the virtual ground node VG of the output supply circuit, i.e. the four "low-side drivers" LSD1, LSD2, LSD3 and LSD4, are represented as a whole by the block labelled "power drivers", which has six respective output terminals HSD1, HSD2, LSD1 ... LSD4, whereby any one of the supply schemes for single or multiple loads depicted in Figures 1a, ... 1d, may be implemented. In the particular example shown in Fig. 2, it is easily recognized that the implemented supply scheme is the one used for controlling an electromagnet. The load L is connected between the two "high-side drivers" and the four "lowside drivers", which are respectively connected in parallel by means of the indicated external connections.

The integrated device has preferably an external terminal VG for allowing the connection of an external sensing resistance Rsense between such a virtual ground terminal VG and the real ground of the circuit powering the external load L.

Naturally the six power switching devices will have customarily a respective integrated diode for recirculation, as shown in Figures 1a, 1b, ... 1d.

The voltage signal across the sensing resistor Rsense is fed to a PWM block wherein such a signal is detected and compared with a control reference voltage Vref and a pulse-width-modulation control circuit generates at least a control signal IN1, the frequency and "duty-cycle" of which may be adjusted by means of said control reference voltage Vref and the Clock signal. The signal (or the two nonsuperimposing driving signals which are needed in case a dual-half-bridge supply scheme for two distinct loads or a supply scheme for a unipolar motor utilizing a single sensing resistor and a single PWM control loop as described in the above cited pending application are implemented) is not fed directly or through inverters to the respective driving terminals of the six output power switching devices but such a driving signal (or two nonsuperimposing driving signals) is fed to an input of a logic circuit labelled ROM - PLA which may be configured by programming and which generates on at least six output terminals thereof, signals which are replica and inverse signals of such a single signal IN1 (or of two nonsuperimposing signals) which is generated by the PWM control loop. The output signals (CA, CB, C0, C1, C2 and C3) of the configurable logic circuit (ROM - PLA) are respectively fed to the six driving terminals of the output power drivers. The configurable logic circuit (ROM -PLA) is provided with at least a first register R1 for the selection of the driving configuration of the external load, which is connected

(obviously in conformity with such a selected configuration) to the relative output terminals of the integrated circuit, a second register R2 for controlling the driving conditions of the load thus connected and preferably a read-only memory (ROM) capable of storing the data of the two registers and/or a logic circuit array whose configuration may be programmed (PLA) and/or equivalent combinatory logic circuitry and determines a configuration of said six output signals in conformity with the data stored in said two registers R1 and R2.

In view of the fact that especially when using ROM and/or PLA having a relatively long access time, the delays imputable to the access time of the programmable circuits may interfere with a correct driving in a switching mode of the external load or loads, an embodiment as the one depicted in Figures 3 and 4 which is particularly suited when the fabrication technology is such as to determine relatively long access times for ROM and for PLA, may be preferred.

As schematically shown in Fig. 3, the function of selecting the configuration of the six output terminals CA, CB, C0, C1, C2 and C3 of the configurable logic circuit is performed by utilizing six "speed-up" circuits, identified by H1, H2, L1, ... L4, respectively. Each block is formed by an AND gate followed by an EX-OR gate as depicted in Fig. 4. A first signal of a pair of signals coming from the ROM is fed to an input terminal of the AND gate of the speed-up circuits as a "forcing" signal of a respective logic state and the second is fed to an input terminal of the EX-OR gate of the speed-up circuits as a "selection of inversion" signal. According to this preferred embodiment the use of relatively slow programmable arrays for implementing the read-only-memory function of the integrated circuit of the invention is made possible.

A more detailed diagram of the circuit of the invention according to such a particularly preferred embodiment, is depicted in Fig. 5.

In the example shown in Fig. 5, the six integrated power switching devices: HSD1, HSD2, LSD1, LSD2, LSD3 and LSD4, provided with their respective recirculation diodes, are clearly shown. Each power switching device commutes a respective output terminal either to the supply rail Vs or to the virtual ground node VG. In the example shown a single external sensing resistor Rsense is connected between the virtual ground node VG and the ground of the supply circuit of one or more external loads (not shown in this figure) which will be connected to the appropriate output terminals, in accordance with a selected supply scheme. Each power switching device is driven by a signal coming respectively from the outputs terminals CA, CB, C0, C1, C2 and C3 of the programmable logic circuit, as clearly shown.

The voltage signal present across the sensing resistor Rsense, by means of the shown connection, and the control signals Vref and Clock are fed to a PWM control circuit of a substantially customary type. The control signal IN1 produced by the PWM control circuit is fed to the input of a speed-up, "flexibility bridge" circuit BFG, one function of which is that of allowing to control a number of half-bridge circuits, eventually coupled among them in a bridge configuration, thus permitting to control the driving by means of a single control signal IL or IR (assuming that a "low-side driver" is always inverting in respect to the respective "high-side driver" as it is easily understood by a skilled technician), because by considering for example a single left-hand half-bridge (formed by HSD1, LSD1 and LSD2 of the scheme depicted in Fig. 1b) the control signal IL will always be a function of the signal IN1 or of the inverse of the latter; i.e. always "high" or always "low", and therefore the AND gate followed by and EX-OR gate of the BFG circuit will control the function: IL = S (IN1) through the respective left-phase (PL) and left- inversion (XL) signals coming from the ROM. Obviously the same type of control is duplicated by the BFG circuit through the respective PR and XR signals coming from the ROM for generating an IR driving signal for an eventual right-hand half-bridge (formed by HSD2, LSD3 and LSD4 in Fig. 1b). An advantage of such a solution is represented by the small number of components which are necessary for implementing the double half-bridge control as well as by the possibility offered of employing a very slow ROM, because the delay between the signal IN1 generated by the PWM control circuit and the control signals IL and/or IR remains always extremely small, as already observed in relation to the more general schemes of Figures 3 and 4.

As it will be evident to the skilled technician, in case a "full-bridge" supply scheme is utilized, the functions of the "current sharing" CS block are no longer required and the signal "CS disable" coming from the ROM will assume a logic value equivalent to "1" such as to disable the two OR output gates of the CS block. In case a "dual-half-bridge" or a "unipolar motor" supply scheme is selected, the "CS disable" signal will assume a "ø" logic value and the two output signals of the current sharing control circuit "CSC", "IL enable" and "IR enable", are fed to the respective inputs of the two AND gates. The output signals of the two AND gates: IL and IR, essentially correspond to the signals PA and PB of the circuit depicted in Fig. 4 of the cited prior application Serial Number 245,657 of September 16, 1988, so as the "IL enable" and "IR enable" signals correspond sustantially to the two signals Qz and $\overline{Qz}$ of that circuit.

In case a bridge scheme is selected, the two output signals IL and IR of the two AND gates are fed in a replica and in an inverse form, through the shown inverters, to a lag time generating circuit "RTL", i.e. to a circuit capable of determining a certain delay in the transfer of a positive ramp, which circuit has the function of positively excluding simultaneous conduction

of a "high-side driver" and of a respective "low-side driver", according to a common technique.

The pair or the pairs of signals, IL' and $\overline{IL'}$ and IR' and $\overline{IR'}$, respectively, are fed through a multiplexer "MX" to the respective driving terminals of the power switching devices, as it will be described further on.

In case a unipolar-motor mode of operation is selected by means of the register R1 (Fig. 1d scheme), the four control phases (phase 1, 2, 3 and 4) are set by means of the register R2 and through the shown connections these signals are fed to the respective inputs of the multiplexer MX to which also the two control signals IR and IL generated as described before by means of the PWM control circuit, the CS current sharing circuit and the BFG circuit are fed. By means of the "unipolar/bridge select" signal coming from the ROM, the multiplexer MX is preset and the six driving signals CA, CB, C3, C2, C1 and C0 for the respective six power switching devices are enabled by means of two enable/disable signals, respectively "R enable" and "L enable" also coming from ROM and which, by means of the six AND gates connected on the six outputs of the multiplexer MX permit to force to an OFF state (disable) the driving signals.

The use of the multiplexer MX is particularly effective for performing a selection among bridge type and unipolar-motor type supply schemes which are radically different from each other and this allows to reduce the number of components which are required for implementing the programmable logic circuitry which is employed in the integrated device of the present invention.

The driving signals relating to the implementation of a bridge type supply scheme or of a solenoid control, are grouped in Fig. 5 by the label "bridge drive signals", while the ensemble of driving signals relating to the implementation of a unipolar-motor supply scheme are labelled "unipolar drive signals" in the diagram of the same Fig. 5.

Notwithstanding the fact that only few preferred embodiments of the invention have been illustrated wherein a ROM is employed, it will be evident to the skilled technician that the ROM may also be substituted by an equivalent logic circuit such as for example a programmable logic array (PLA, PAL, etc.) or by equivalent combinatory logic circuitry. Moreover the invention may be practiced in different embodiments, modified in respect to the embodiments which have been described herein for purely illustrative purposes.

Claims

1. An integrated circuit for driving in a switching mode one or more external loads connected, in accordance with a certain supply scheme, to output terminals (HSD1, HSD2, LSD4, LSD3, LSD2, LSD1) of the integrated circuit which essentially comprise at least one or optionally two high-side driver, power switching integrated devices (HSD1, HSD2) having a common terminal connected to a supply rail, four low-side driver, power switching integrated devices (LSD1, LSD2, LSD3, LSD4) having a common terminal connected to a virtual ground node (VG) of the integrated circuit, a second terminal of each of said integrated power switching devices being connected respectively to one of an equal number of output terminals of the integrated circuit, an external sensing resistor (Rsense) being connected between said virtual ground node and a real ground node of the supply circuit, each of said integrated power switching devices having a control terminal to which a driving signal is fed, means for detecting and comparing a signal present across said sensing resistor (Rsense) with a control reference voltage (Vref), at least a pulse-width-modulation (PWM) control circuit capable of generating a control signal having a frequency and a duty-cycle respectively controlled by means of a clock signal (clock) and said control reference voltage (Vref), capable of selecting among different bridge and unipolar-motor modes of operation characterized by comprising:

a first register (R1) for selecting a certain connection scheme of an external load that is connected, in conformity with said selected scheme, to said output terminals of the integrated circuit;

a second register (R2) for controlling the driving conditions of said externally connected load;

a read-only memory (ROM) or equivalent logic circuit producing a configuration of output signals (PL, PR, XL, XR) for conditioning a combinatory logic circuit (BFG, CS) in conformity with data stored in said first (R1) and said second (R2) registers;

a combinatory logic circuit (BFG, CS) receiving said control signal generated by said PWM control circuit and said conditioning signals (PL, PR, XL, XR) output by said ROM and producing driving signals (IR, IL) and through a delay circuit (RTL) delayed, complementary driving signals (IR', IL', $\overline{IR'}$, $\overline{IL'}$) as a function of said control signal generated by said (PWM) control circuit, in conformity with said configuration of output signals produced by said read-only-memory;

at least a multiplexer circuit (MX) selecting between bridge type and unipolar-motor type driving mode as a function of a conditioning (Unipolar/Bridge Select.) output signal produced by said ROM and transferring said driving signals produced by said combinatory logic circuit (BFG, CS) and delaying and inverting circuit (RTL) to

output terminals thereof which are operatively connected to said control terminals of said integrated power switching devices through enabling/disabling means (CA, CB, C0, C1, C2, C3) controlled by enable/disable signals (Renable, Lenable) output by said ROM.

2. The circuit according to claim 1, wherein said enabling/disabling means (CA, CB, C0, C1, C2, C3) cascaded from the outputs of said multiplexer (MX) comprise an equal number of logic AND gates cascaded respectively therefrom, each being capable of receiving through a first input terminal the signal coming from one of said output terminals of said multiplexer (MX) and, through a second input terminal, an enable/disable signal (Renable/Lenable) coming from said ROM and to transfer while in an enable condition, through an output terminal a driving signal to the control terminal of a respective integrated power switching device (HSD1, HSD2, LSD1, LSD2, LSD3, LSDS4).

Patentansprüche

1. Integrierte Schaltung zum Treiben einer oder mehrerer externer Lasten in einem Schaltmodus, welche Lasten gemäß einem gewissen Speiseschema an Ausgangsanschlüsse (HSD1, HSD2, LSD4, LSD3, LSD2, LSD1) der integrierten Schaltung angeschlossen sind, die im wesentlichen mindestens einen oder - optional - zwei hochpotentialseitige, integrierte Treiber-Leistungsschaltelemente (HSD1, HSD2), die mit einem gemeinsamen Anschluß an eine Versorgungsspannungsschiene angeschlossen sind, vier niedrigpotentialseitige, integrierte Treiber-Leistungsschaltelemente (LSD1, LSD2, LSD3, LSD4), die mit einem gemeinsamen Anschluß an einen virtuellen Masseknoten (VG) der integrierten Schaltung angeschlossen sind, aufweisen, wobei ein zweiter Anschluß jedes der integrierten Leistungsschaltelemente an einen von einer gleichen Anzahl von Ausgangsanschlüssen der integrierten Schaltung angeschlossen ist, ein externer Fühlwiderstand (Rsense) zwischen den virtuellen Masseknoten und einen realen Masseknoten der Speiseschaltung geschaltet ist, jedes der integrierten Leistungsschaltelemente einen Steueranschluß aufweist, dem ein Treibersignal zugeführt wird, Mittel vorgesehen sind, um ein an dem Fühlwiderstand (Rsense) vorhandenes Signal zu erfassen und mit einer Steuer-Bezugsspannung (Vref) zu vergleichen, mindestens eine Pulsbreitenmodulations-(PWM-)Steuerschaltung in der Lage ist, ein Steuersignal mit einer Frequenz und einem Tastverhältnis zu erzeugen, die jeweils mittels eines Taktsignals (Takt) und der Steuer-Bezugsspannung (Vref) gesteuert werden, und die in der Lage ist, zwischen unterschiedlichen Brücken- und Unipolar-Motor-Betriebsarten auszuwählen, gekennzeichnet durch:
ein erstes Register (R1) zum Auswählen eines gewissen Verbindungsschemas der externen Last, die konform mit dem ausgewählten Schema an die Ausgangsanschlüsse der integrierten Schaltung angeschlossen wird;
ein zweites Register (R2) zum Steuern der Treiberbedingungen für die extern angeschlossene Last;
einen Festspeicher (ROM) oder eine diesem äquivalente logische Schaltung zum Erzeugen einer Konfiguration von Ausgangssignalen (PL, PR, XL, XR) zum Konditionieren einer Kombinatorik-Logikschaltung (BFG, CS) in Einklang mit in dem ersten (R1) und dem zweiten (R12) Register gespeicherten Daten;
eine Kombinatorik-Logikschaltung (BFG, CS), die das von der PWM-Steuerschaltung erzeugte Steuersignal und die Konditioniersignale (PL, PR, XL, XR), die von dem ROM ausgegeben werden, empfängt und Treibersignale (IR, IL) sowie durch eine Verzögerungsschaltung (RTL) verzögerte, komplementäre Treibersignale (IR', IL', $\overline{IR}$', $\overline{IL}$') als Funktion des von der PWM-Steuerschaltung erzeugten Steuersignals in Einklang mit der Konfiguration der von dem Festspeicher erzeugten Ausgangssignale erzeugt;
mindestens eine Multiplexerschaltung (MX) zum Auswählen zwischen einer Brücken-Typ- und einer Unipolar-Motor-Typ-Treiberbetriebsart als Funktion eines von dem ROM erzeugten Konditionier-Ausgangssignals (Unipolar/Brükken-Auswahl), und zum Transferieren der von der Kombinatorik-Logikschaltung (BFG, CS) und der Verzögerungs- und Invertierschaltung (RTL) erzeugten Treibersignale an deren Ausgangsanschlüsse, die betrieblich mit den Steueranschlüssen der integrierten Leistungsschaltelemente über Freigabe-/Sperr-Mittel (CA, CB, C0, C1, C2, C3) verbunden sind, welche von Freigabe-/Sperr-Signalen (Renable, Lenable) gesteuert werden, welche von dem ROM ausgegeben werden.

2. Schaltung nach Anspruch 1, bei der die Freigabe-/Sperr-Einrichtung (CA, CB, C0, C1, C2, C3), die an die Ausgänge des Multiplexers (MX) anschließen, eine gleichgroße Anzahl logischer UND-Gatter aufweist, welche jeweils daran anschließen, und die jeweils in der Lage sind, über einen ersten Eingangsanschluß das von einem der Ausgangsanschlüsse des Multiplexers (MX) kommende Signal und über einen zweiten Eingangsanschluß ein von dem ROM kommendes Freigabe-/Sperr-Signal (Renable, Lenable) zu

empfangen, um in einem Freigabezustand über einen Ausgangsanschluß ein Treibersignal an den Steueranschluß eines zugehörigen integrierten Leistungsschaltelements (HSD1, HSD2, LSD1, LSD2, LSD3, LSD4) zu übermitteln.

Revendications

1. Circuit intégré pour commander en mode à découpage une ou plusieurs charges externes connectées selon un certain schéma d'alimentation à des bornes de sortie (HSD1, HSD2, LSD4, LSD3, LSD2, LSD1) du circuit intégré qui comprend essentiellement au moins un ou optionnellement deux dispositifs intégrés de commutation de puissance de type "dispositif de commande supérieur" (HSD1, HSD2) ayant une borne commune connectée à un rail d'alimentation, quatre dispositifs intégrés de commutation de puissance de type "dispositif de commutation inférieur" (LSD1, LSD2, LSD3, LSD4) ayant une borne commune connectée à un noeud de masse virtuelle (VG) du circuit intégré, une seconde borne de chacun des dispositifs intégrés de commutation de puissance étant connectée respectivement à l'une de bornes de sortie en nombre égal du circuit intégré, une résistance de détection externe (Rsense) étant connectée entre le noeud de masse virtuelle et un noeud de masse réelle du circuit d'alimentation, chacun des dispositifs intégrés de commutation de puissance ayant une borne de commande à laquelle est fourni un signal de commande, des moyens pour détecter et comparer un signal présent aux bornes de la résistance de détection (Rsense) à une tension de référence (Vref), au moins un circuit de commande de modulation de largeur d'impulsion (PWM) capable de produire un signal de commande ayant une fréquence et un rapport cyclique respectivement commandés par un signal d'horloge (Clock) et la tension de référence de commande (Vref), capable de sélectionner entre différents modes de fonctionnement en pont et en moteur unipolaire, caractérisé en ce qu'il comprend :

un premier registre (R1) pour sélectionner un certain schéma de connexion d'une charge externe qui est connectée, conformément au schéma choisi, aux bornes de sortie du circuit intégré ;

un second registre (R2) pour commander les conditions d'alimentation de la charge connectée de façon externe ;

une mémoire morte (ROM) ou un circuit logique équivalent produisant une configuration de signaux de sortie (PL, PR, XL, XR) pour conditionner un circuit logique combinatoire (BFG, CS) en conformité avec des données mémorisées dans les premier (R1) et second (R2) registres ;

un circuit logique combinatoire (BFG, CS) recevant le signal de commande produit par le circuit de commande PWM et les signaux de conditionnement (PL, PR, XL, XR) fournis par la ROM et produisant des signaux de commande (IR, IL) et, par l'intermédiaire d'un circuit de retard (RTL), des signaux de commande complémentaires retardés (IR', IL' $\overline{IR'}$, $\overline{IL'}$) en fonction du signal de commande produit par le circuit de commande (PWM), en conformité avec la configuration des signaux de sortie produits par ladite mémoire ROM ;

au moins un circuit multiplexeur (MX) sélectionnant entre un mode d'alimentation de type pont et de type moteur bipolaire en fonction d'un signal de sortie de conditionnement (Sélection unipolaire/pont) produit par la ROM et transférant les signaux de commande produits par le circuit logique combinatoire (BFG, CS) et un circuit de retard et d'inversion (RTL) à des bornes de sortie qui sont opérativement connectées aux bornes de commande des dispositifs de commutation de puissance intégrés par l'intermédiaire de moyens de validation/invalidation (CA, CB, C0, C1, C2, C3) commandés par des signaux de validation/invalidation (Renable, Lenable) fournis par la ROM.

2. Circuit selon la revendication 1, dans lequel les moyens de validation/invalidation (CA, CB, C0, C1, C2, C3) cascadés à partir des sorties du multiplexeur (MX) comprennent un nombre égal de portes logiques ET respectivement cascadées à partir de là, dont chacune peut recevoir par une première borne d'entrée le signal provenant de la première des bornes de sortie du multiplexeur (MX) et, par l'intermédiaire d'une seconde borne d'entrée, un signal de validation/invalidation (Renable/Lenable) provenant de la ROM et transférer, quand on est dans l'état de validation, par une borne de sortie, un signal de commande à la borne de commande d'un dispositif de commutation de puissance intégré respectif (HSD1, HSD2, LSD1, LSD2, LSD3, LSD4).

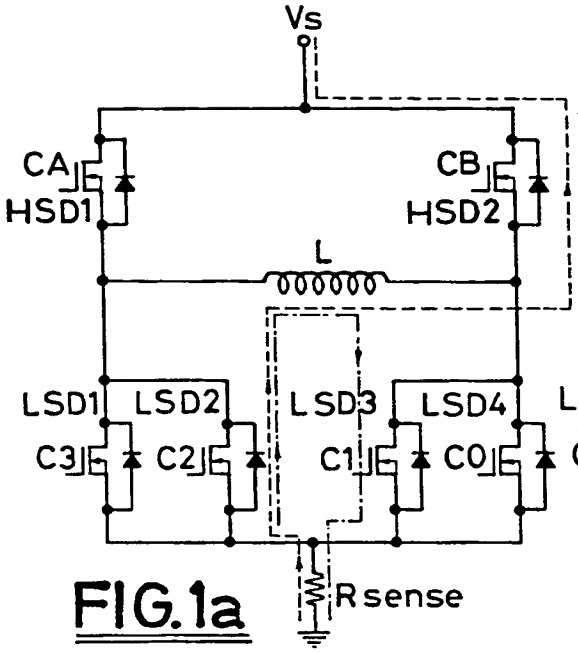

FIG.1a

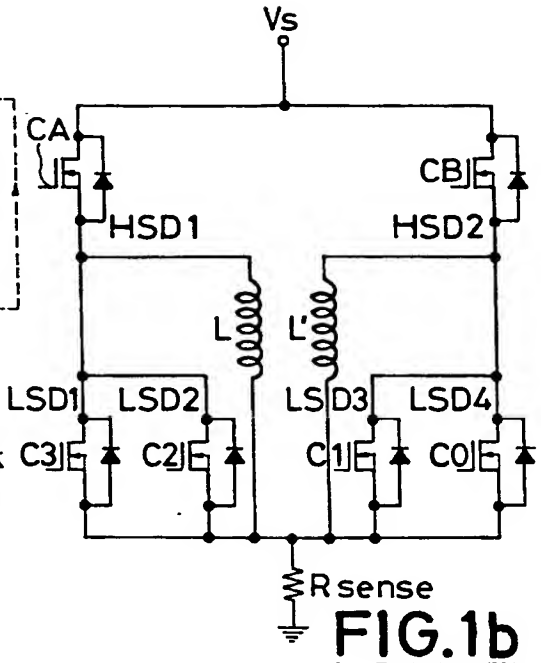

FIG.1b

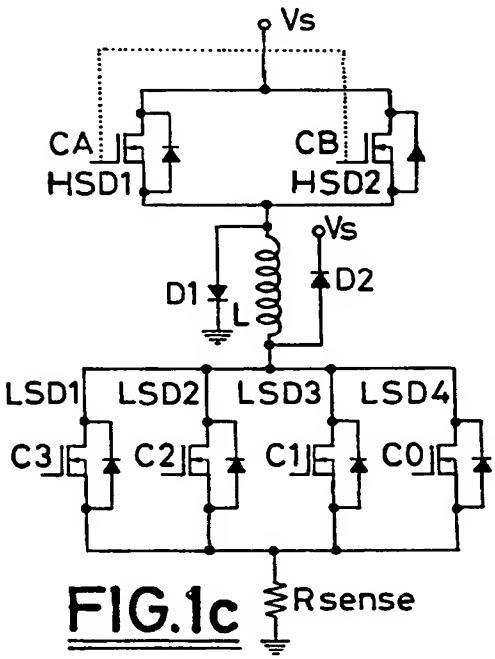

FIG.1c

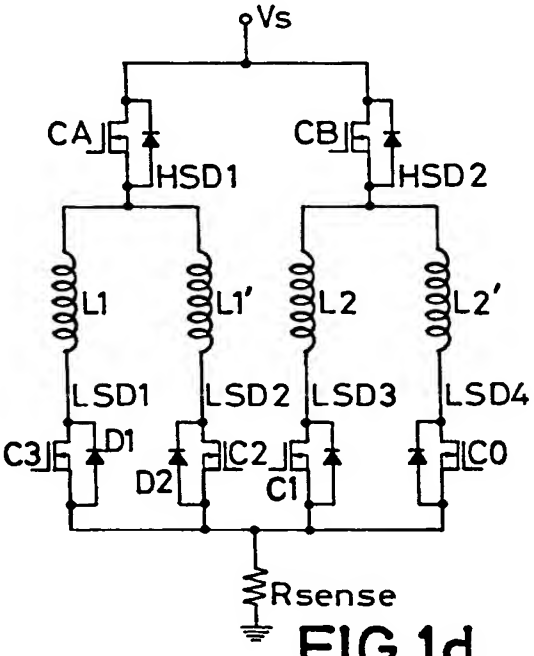

FIG.1d

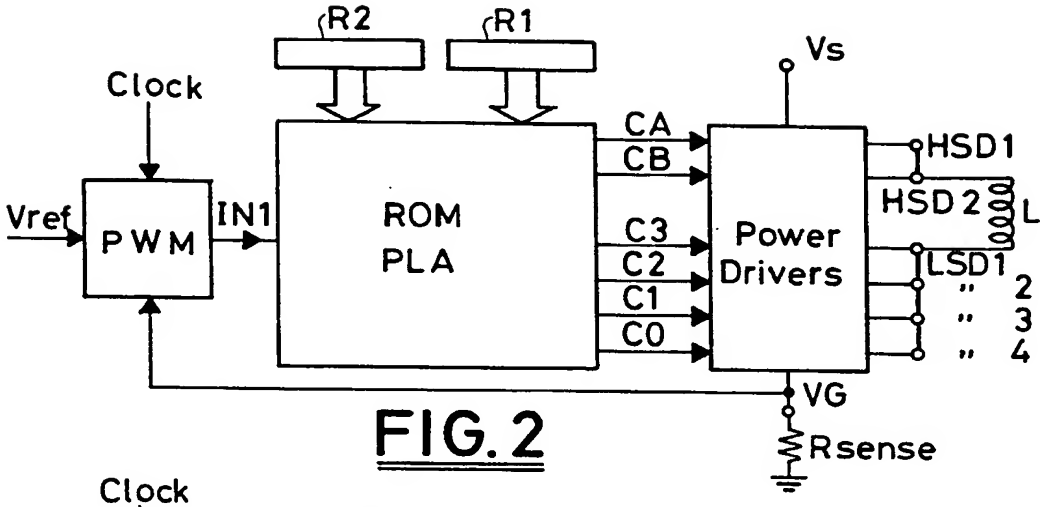

FIG. 2

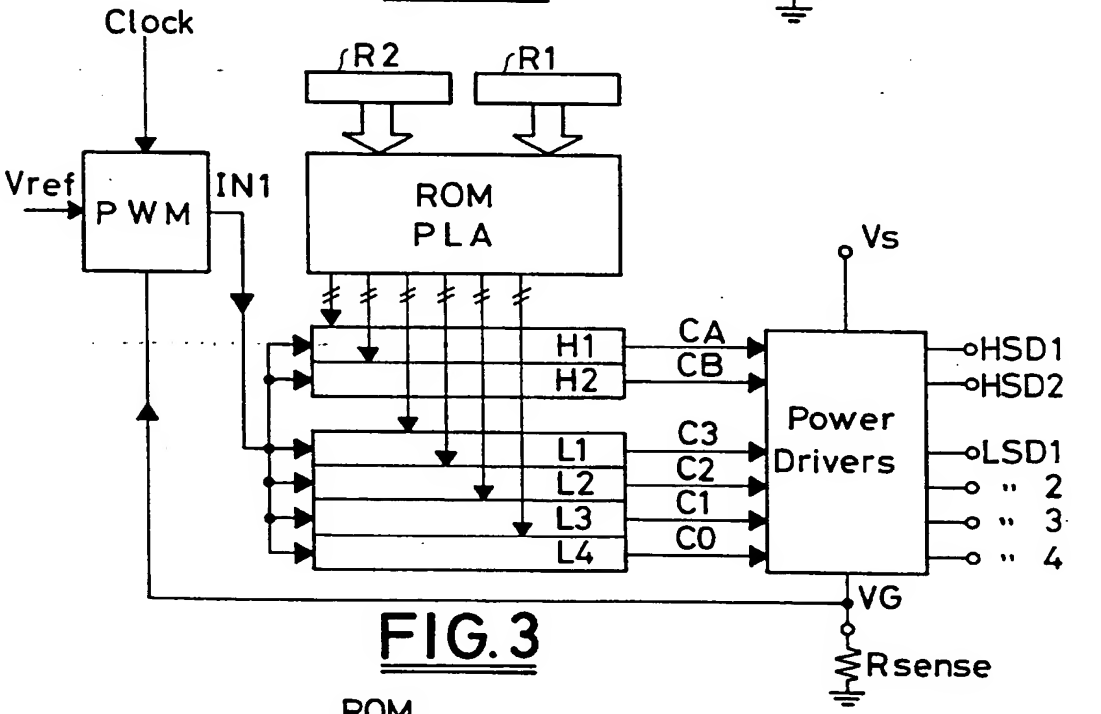

FIG. 3

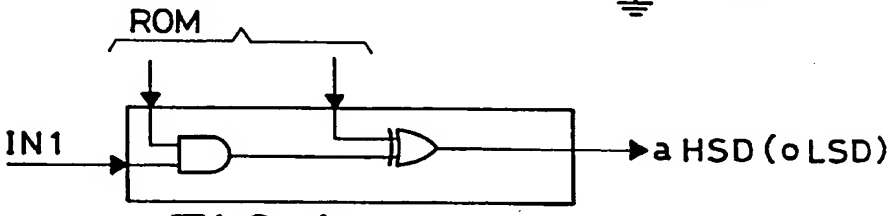

FIG. 4

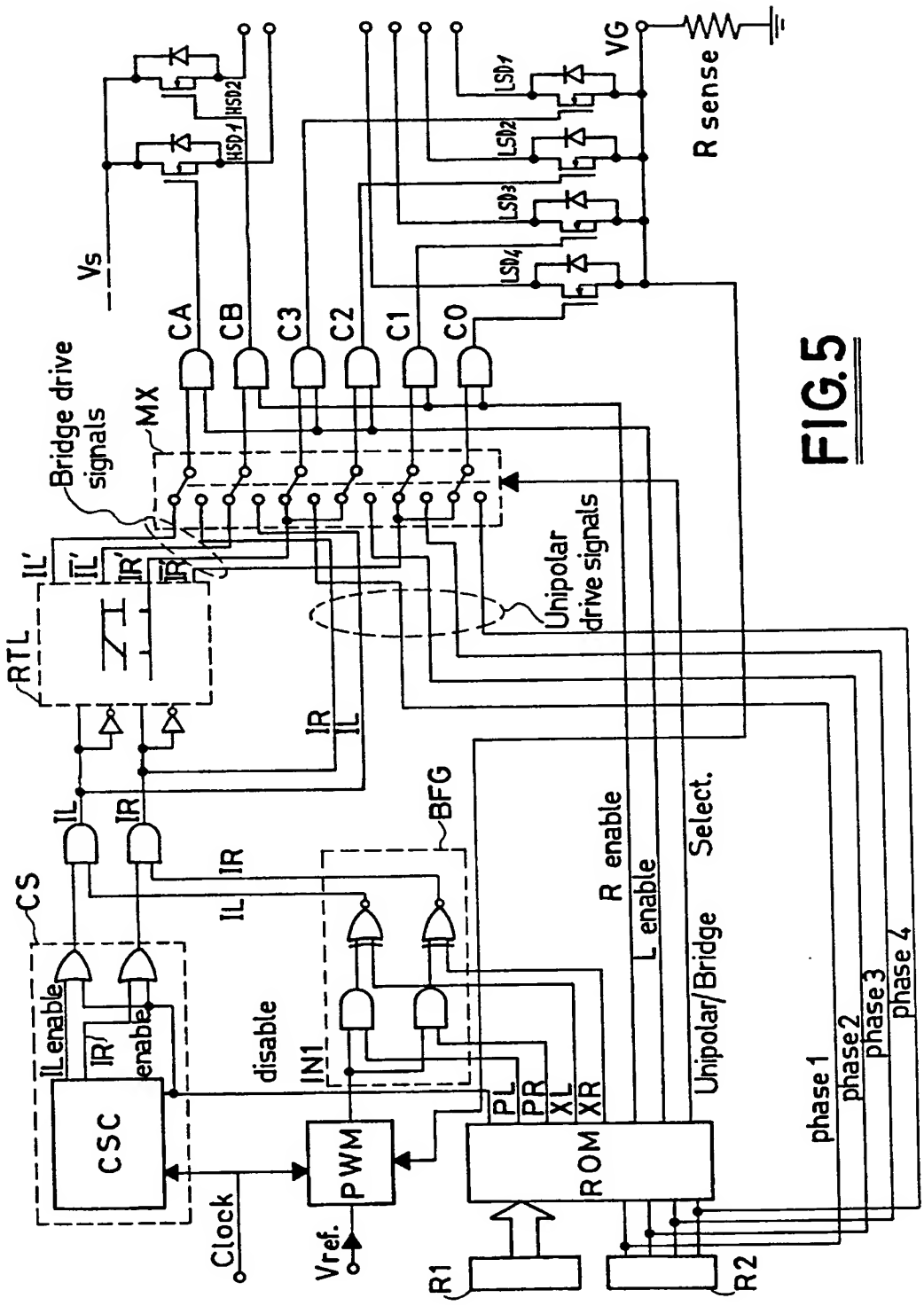
VG
R sense
LSD1
LSD2
LSD3
LSD4
HSD1
HSD2
Vs
CA
CB
C3
C2
C1
C0
MX
Bridge drive signals
Unipolar drive signals
IL'
IR'
RTL
IR
IL
BFG
R enable
L enable
Select.
Unipolar/Bridge
CS
IL enable
IR' enable
disable
IN1
PL
PR
XL
XR
CSC
PWM
ROM
Clock
Vref.
R1
R2
phase 1
phase 2
phase 3
phase 4

FIG.5